CEN 305 MIPS Single Cycle Processor Project Description

In this project, you will implement a single cycle MIPS processor. Your processor should provide add, sub, and, or, lw, sw and beq. Besides this you should provide addi instruction. You should both provide Max2Plus implementation and the waveform test files. The milestones of the projects are listed below (Each item listed below will be demonstrated in your regular lab hour unless otherwise stated):

BRD: Brief Report Delivery about the study

1. December 2nd week: ALU Design and BRD
2. December 3rd week: Instruction Memory / Data Memory and BRD
3. December 4th week: Control Unit and BRD
4. January 1st week: Register File and BRD
5. 20.January.2012:
    - Integration of CPU components and demonstration of the sample code given below.
    - A comprehensive report consisting of brief reports including the integration.

To test your implementation, you should implement the below source code:

```
addi $2,$0,2
addi $5,$0,5
addi $3,$0,3
or $8,$0,$2
sw $8, 2($5)
lw $7,2($5)
sub $3,$5,$3
beq $2,$3,bypass
add $3,$3,$3
bypass: add $3,$3,$2
```