



**Question 2 (Pipeline Forwarding).** Show all the data hazards in this code.

Please define the hazards in this format:

Example: EX/MEM hazard between instructions 3 and 4, because register rs=3 and register rd=3.

1. add \$8, \$2, \$3
2. sub \$6, \$8, \$7
3. or \$3, \$1, \$8
4. add \$5, \$3, \$6
5. sub \$1, \$5, \$6
6. and \$4, \$5, \$5

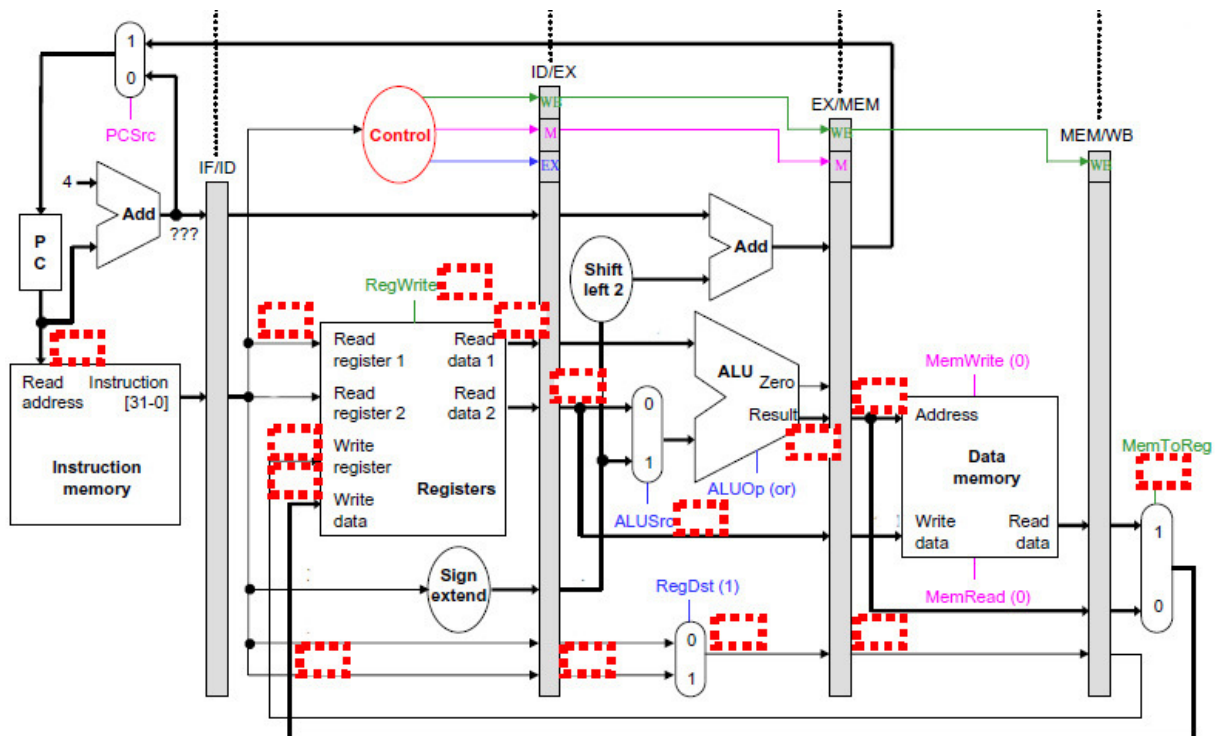
**Question 3 (MIPS Pipelined CPU).** Here's a sample sequence of instructions to execute.

- 1000: lw \$30, 29(\$28)
- 1004: and \$27, \$26, \$25
- 1008: or \$24, \$23, \$22
- 1012: sub \$21, \$20, \$19
- 1016: add \$18, \$17, \$16

— Each register contains its number plus 100. For instance, register \$8 contains 108, register \$29 contains 129, and so forth.

— Every data memory location contains 99.

Please fill the values into the boxes at the fifth cycle.



Notes:

1. Please do not submit it as a homework.
2. Please restudy Homework 1 and Homework 2.

Assit. Prof. Dr. Orhan Dagdeviren